What is claimed is:

[Claim 1] 1. A method of fabricating a heterobipolar transistor comprising:

forming a pedestal atop a structure that comprising at least a base layer located on a surface of a substrate having a collector and trench isolation regions located therein, wherein said base layer is monocrystalline over the collector and polycrystalline over the trench isolation regions;

forming an extra base layer over said structure including said pedestal, wherein said extra base layer comprises monocrystalline material over the substrate and polycrystalline material over the pedestal and said base layer that is polycrystalline, said polycrystalline material over said pedestal is thinner than the polycrystalline material over said base layer that is polycrystalline;

converting at least said polycrystalline material over said pedestal of said extra base layer into an oxide utilizing a low temperature process that is performed at a temperature of about 700°C or less;

removing said oxide and said pedestal from said structure to provide an emitter opening; and

forming at least a polysilicon emitter in said emitter opening.

[Claim 2] 2. The method of Claim 1 wherein said pedestal is an oxide pedestal that is formed by deposition, lithography and etching.

[Claim 3] 3. The method of Claim 2 wherein said removing of said oxide formed by said converting step and said oxide pedestal are performed using a single etching step and some polycrystalline material of said extra base layer remains.

[Claim 4] 4. The method of Claim 3 further comprising forming an oxide layer in at least said emitter opening after said removal step.

[Claim 5] 5. The method of Claim 4 wherein said oxide layer is formed by a low temperature oxidation process that is performed at a temperature of about 700°C or less.

[Claim 6] 6. The method of Claim 5 wherein said low temperature oxidation is a high-pressure oxidation process that is performed at a pressure of about 1 atmosphere or greater.

[Claim 7] 7. The method of Claim 4 further comprising forming a nitride spacer on each exposed sidewall within said emitter opening.

[Claim 8] 8. The method of Claim 7 further comprising performing a chemical oxide removal process to remove said oxide layer from a bottom surface of said emitter opening thereby exposing the base layer.

[Claim 9] 9. The method of Claim 8 wherein said chemical oxide removal process is a vapor or a plasma of HF and NH_3.

[Claim 10] 10. The method of Claim 1 wherein said base layer is formed by an epitaxy growth process that is performed at a temperature from about 450°C to about 700°C.

[Claim 11] 11. The method of Claim 1 wherein said base layer comprises Si, SiGe or a combination of Si and SiGe.

[Claim 12] 12. The method of Claim 1 wherein said structure further comprises an optional Si-containing cap layer located atop said base layer.

[Claim 13] 13. The method of Claim 1 wherein said forming said extra base layer comprising an epitaxy growth process that is performed at a temperature from about 450°C to about 700°C.

[Claim 14] 14. The method of Claim 1 wherein said extra base layer comprises Si, SiGe or a combination of Si and SiGe.

[Claim 15] 15. The method of Claim 1 wherein said low temperature oxidation process comprises a high-pressure oxidation process that is performed at a pressure of about 1 atmosphere or greater.

[Claim 16] 16. The method of Claim 1 wherein said removing step comprises an etching process that selectively removes oxide.

[Claim 17] 17. The method of Claim 1 wherein said forming at least said polysilicon emitter comprising depositing a doped or undoped polysilicon layer, optionally implanting dopants into said undoped polysilicon layer, lithography and etching.

[Claim 18] 18. The method of Claim 1 wherein said pedestal comprising a nitride located atop an oxide base layer.

[Claim 19] 19. The method of Claim 18 wherein said pedestal is formed by providing an oxide base layer, forming a nitride layer on said oxide base layer, lithography and etching.

[Claim 20] 20. The method of Claim 18 wherein said removing said oxide and said pedestal containing nitride are performed in separate etching steps, wherein said oxide is first removed exposing said pedestal containing nitride and then said pedestal containing nitride is removed exposing said oxide base layer.

[Claim 21] 21. The method of Claim 20 further comprising performing a low temperature oxidation process after removing said oxide whereby an oxide layer is formed on surfaces not including said pedestal containing nitride.

[Claim 22] 22. The method of Claim 20 further comprising forming nitride spacers on said exposed oxide base layer.

[Claim 23] 23. The method of Claim 22 further comprising a chemical oxide removal process which selectively removes said exposed oxide base layer.

[Claim 24] 24. A method of forming a heterobipolar transistor comprising the steps of:

forming an oxide pedestal atop a structure that comprising at least a base layer located on a surface of a substrate having a collector and trench isolation regions located therein, wherein said base layer is monocrystalline over the collector and polycrystalline over the trench isolation regions;

forming an extra base layer over said structure including said oxide pedestal, wherein said extra base layer comprises monocrystalline material over the substrate and polycrystalline material over the oxide pedestal and said base layer that is polycrystalline, said polycrystalline material over said oxide pedestal is thinner than the polycrystalline material over said base layer that is polycrystalline;

converting at least said polycrystalline material over said oxide pedestal of said extra base layer into an oxide utilizing a low temperature oxidation process;

removing said oxide and said oxide pedestal from said structure using a single etching process to provide an emitter opening;

forming an oxide layer on exposed surfaces using a second low temperature oxidation process;

forming a nitride spacer within said opening;

removing said oxide layer from a bottom surface of said emitter opening exposing said base layer; and

forming at least a polysilicon emitter in said emitter opening.

[Claim 25] 25. A method of forming a heterobipolar transistor comprising the steps of:

forming a nitride pedestal atop on oxide base, said oxide base is located on a structure that comprising at least a base layer located on a surface of a substrate having a collector and trench isolation regions located therein, wherein said base layer is monocrystalline over the collector and polycrystalline over the trench isolation regions;

forming an extra base layer over said structure including said nitride pedestal, wherein said extra base layer comprises monocrystalline material over the substrate and polycrystalline material over the nitride pedestal and said base layer that is polycrystalline, said polycrystalline material over said nitride

pedestal is thinner than the polycrystalline material over said base layer that is polycrystalline;

converting at least said polycrystalline material over said nitride pedestal of said extra base layer into an oxide utilizing a low temperature oxidation process;

removing said oxide from said structure to form a partial emitter opening;

performing a second low temperature oxidation process to provide an oxide layer outside said partial emitter opening;

removing said nitride pedestal exposing said oxide base in said partial emitter opening to provide an emitter opening;

forming a nitride spacer within said emitter opening;

removing said oxide layer from a bottom surface of said emitter opening exposing said base layer; and

forming at least a polysilicon emitter in said emitter opening.

[Claim 26] 26. A heterobipolar transistor comprising:

a semiconductor substrate including a collector;

a base region located atop said collector;

an extra base region located atop said base region, said extra base region comprises at least a single crystalline area above said collector and periphery regions that include polycrystalline or single crystalline material; and

an emitter region located above said single crystal area of said extra base region, wherein said periphery regions of said extra base region are self aligned to edges of emitter region and contain an oxide layer thereon.